REMARKS

Claims 1 and 3-14 are pending in the application. Claim 1 has been amended by the present amendment to recite that each of the interposer units is formed with a solder mask having a plurality of openings and a plurality of test pads exposed via the openings of the solder mask. Claim 10 has been amended to properly agree with claim 1. The amendments are fully supported by the application as originally filed (see specification at page 7, fourth paragraph; FIG. 2C).

Applicant's claimed invention is directed to a wafer test method including a conductive interposer disposed between and electrically connected to a wafer and test probes, in order to prevent the test probes from directly contacting and damaging bond pads on the wafer during a test.

For example, as shown in FIG. 2C, a first surface of each interposer unit (of the conductive interposer) is formed with a solder mask 39 having a plurality of openings 390 and a plurality of test pads 33 exposed via the openings of the solder mask 39, such that the test probes contact the exposed test pads 33 to perform a test on the wafer (see specification at page 7, fourth paragraph).

Claims 1 and 3-14 were rejected under 35 USC 102(b) as being anticipated by U.S. Patent 5,559,446 to Sano. This rejection is respectfully traversed.

Sano does not teach or suggest a wafer test method in which a solder mask is formed on the first surface of a conductive interposer, and test pads are exposed via openings in the solder mask.

Referring to FIGS. 1 and 2 of Sano, a probe card 2 or card body 20 "is formed with connecting through holes 22 ... arranged at the outer circumferential portion thereof," so as to be in contact with pogo pins 51 (see column 4, lines 25-30).

As described in column 5, line 16 to column 6, line 3 of Sano, when performing a test, a heater 1 is turned on to heat the wafer W up to 80° to 150°C, and the wafer W and a thin substrate 4 expand at about the same rate, such that a dislocation rate of electrode pads on the wafer W is almost equivalent to that of the bumps 41 on the probe card 2 "to keep the reliable mutual positional relationship with respect to each other."

In other words, Sano addresses a problem in the prior art of positional dislocation between bumps and electrode pads in response to temperature change, e.g., due to a large difference in coefficient of thermal expansion (CTE) between a flexible thin film resin and a silicon wafer. In Sano, as the bumps 41 are dislocated when the thin substrate 4 expands, the connecting through holes 22 would not be formed at an area corresponding to the bumps 41.

On page 4, second paragraph of the Office Action of 08/04/2005, it was alleged that part of the wiring substrate 3 applied over the upper surface of the core 20 in Sano corresponds to Applicant's claimed "solder mask." However, in Sano, the upper surface of wiring substrate 3 is formed with a grounding layer 30 and connecting through holes 22, but **not** with a solder mask.

For at least the reasons discussed above, Sano does not anticipate or otherwise render obvious the Applicant's claimed invention.

It is believed the application is in condition for immediate allowance, which action is earnestly solicited.

Respectfully submitted,

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